Remarks

A. Claims

Claims 1, 2, 6-11, 14-15, 17, 22-24, and 27-31 have been amended. Claims 20-21 have been cancelled. Claims 36-37 have been added. Claims 1-20 and 23-37 are pending.

B. Oath/Declaration

The Examiner indicates that at this time an earlier priority date has not been granted. Applicant respectfully submits the current application does not claim priority to a provisional.

C. 35 U.S.C. §112 Rejections

The Examiner has rejected claim 11 under 35 U.S.C. §112 for improper antecedent basis. Claim 11 has been amended to correct the antecedent basis issue. Applicant respectfully requests the Examiner to withdraw the rejection to claim 11.

D. 35 U.S.C. §102(b) Rejections

The Examiner has rejected claims 15-17, 20-26, and 28-30 under 35 U.S.C. §102(b) as being anticipated by Beardsley et al. (U.S. Patent No. 5,471,631) (hereinafter "Beardsley"). Applicant respectfully disagrees with these rejections.

Applicant respectfully reminds the Examiner that the standard for "anticipation" is one of fairly strict identity. To anticipate a claim of a patent, a single prior source must contain all the claimed essential elements. *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231

U.S.P.Q.81, 91 (Fed.Cir. 1986); *In re Donahue*, 766 F.2d 531, 226 U.S.P.Q. 619, 621 (Fed.Cir. 1985).

Beardsley does not disclose, teach, or suggest at least "determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips" as recited in claim 15. The Examiner points to Beardsley, however, Beardsley discloses:

> In one embodiment of the invention, the predetermined data processing event is a detected error condition in the peripheral subsystem, the data storage system is an error log and the event time stamp and an indication of the error event are stored as one entry of the error log.. The time-correlating entry is stored as a separate entry in such error log. Problem determination includes correlating the recorded error event to the host time of day by calculating the host time of day that correlates to the event time stamp by adding the difference between the host time stamp and the peripheral clock time stamp in the time-correlating entry. (emphasis added) (Beardsley, col. 2, line 62 – col. 3, line 5).

Applicant respectfully submits Beardsley is directed to a "host processor portion" and "peripheral subsystems." Beardsley is not directed towards a processor and a plurality of chips in an electronic device.

In addition, Beardsley does not teach at least "determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips" where "each said chip associated with a local time counter" as recited in claim 15. Applicant respectfully asserts claim 15 and claims dependent thereon are allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claim 15 and claims dependent thereon.

Applicant respectfully disagrees with the Examiner rejection of claims 20-21, however, as claims 20-21 have been cancelled, the rejection is believed moot.

Beardsley also does not disclose, teach, or suggest at least "In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter... generating a timestamp with said local time counter at the time of the occurrence (emphasis added)" as recited in claim 22. Applicant respectfully asserts claim 22 and claims

dependent thereon are allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claim 22 and claims dependent thereon.

Applicant also submits that independent claims 15 and 22 are further non-obvious over the cited art for similar reasons as stated above.

E. 35 U.S.C. § 103(a) Rejections

Claims 1-5 and 7-9

The Examiner has rejected claims 1-5 and 7-9 under 35 U.S.C. §103(a) as being obvious over Beardsley in view of U.S. Patent No. 6,718,476 to Shima (hereinafter "Shima"). Applicant respectfully disagrees with these rejections.

In order to reject a claim as obvious, the Examiner has the burden of establishing a *prima facie* case of obviousness. *In re Warner* et al., 379 F.2d 1011, 154 U.S.P.Q. 173, 177-178 (C.C.P.A. 1967). To establish a *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP § 2143.03.

Neither Beardsley nor Shima disclose, teach, or suggest, either separately or in combination at least "In an isochronous electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter... generating a timestamp with said local time counter (emphasis added)" as recited in claim 1. As stated above, Beardsley is not directed towards a processor and a plurality of chips in an electronic device. The Examiner points to the nodes of Shima, however, Shima states: "Each node is a device (e.g., computer system, digital camera, digital VCR, TV settop box, digital camcorder, storage device, digital audio device... (Shima, col. 7, lines 47-50)." Neither Beardsley nor Shima teach generating timestamps in an electronic device. Applicant respectfully asserts claim 1 and claims dependent thereon are allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claim 1 and claims dependent thereon.

Claims 11-12

The Examiner has rejected claims 11-12 under 35 U.S.C. §103(a) as being obvious over Beardsley in view of Shima in further view of U.S. Patent No. 5,682,551 to Pawlowski et al. (hereinafter "Pawlowski"). Applicant respectfully disagrees with these rejections. Applicant respectfully asserts claims 11-12, dependent on patentably distinct claim 1, are allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claims 11-12.

Claim 13

The Examiner has rejected claim 13 under 35 U.S.C. §103(a) as being unpatentable over Beardsley in view of Shima and further in view of U.S. Patent No. 4,852,095 to Meltzer (hereinafter "Meltzer"). Applicant respectfully disagrees with these rejections. Applicant respectfully asserts claim 13, dependent on patentably distinct claim 1, is allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claim 13.

Claim 14

The Examiner has rejected claim 14 under 35 U.S.C. §103(a) as being unpatentable over Beardsley in view of Shima and further in view of U.S. Patent No. 6,334,191 to Fisher et al. (hereinafter "Fisher"). Applicant respectfully disagrees with these rejections. Applicant respectfully asserts claim 14, dependent on patentably distinct claim 1, is allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claim 14.

Claims 18, 32, and 33

The Examiner has rejected claims 18, 32, and 33 under 35 U.S.C. §103(a) as being unpatentable over Beardsley in view of Pawlowski. Applicant respectfully disagrees with these rejections. Applicant respectfully disagrees with these rejections. Applicant respectfully asserts claims 18, and 32, 33 dependent on patentably distinct claims 15 and 22, respectively, are allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claims 18, 32, and 33.

Claims 19 and 34

The Examiner has rejected claims 19 and 34 under 35 U.S.C. §103(a) as being unpatentable over Beardsley in view of Meltzer. Applicant respectfully disagrees with these rejections. Applicant respectfully asserts claims 19 and 34 dependent on patentably distinct claims 15 and 22, respectively, are allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claims 19 and 34.

Claim 35

The Examiner has rejected claim 35 under 35 U.S.C. §103(a) as being unpatentable over Beardsley in view of Fisher. Applicant respectfully disagrees with these rejections. Applicant respectfully asserts claim 35, dependent on patentably distinct claim 22, is allowable for at least the above reasons. Applicant respectfully requests the Examiner withdraw the rejection to claim 35.

F. Allowable Claims

Claims 6, 10, 27 and 31 have been objected to as dependent on a rejected base claim, but indicated allowable otherwise. Applicant respectfully submits claims 6, 10, 27 and 31 are also at least allowable as dependent on patentably distinct claims 1 and 22.

Applicant respectfully disagrees with the Examiner's Statement of Reasons for

Allowance and/or Applicant believes that the Examiner's Statement of Reasons for Allowance is incomplete.

Applicant respectfully submits that the cited art does not teach or suggest the combinations of features set forth in the Applicant's claims. By way of nonlimiting example, Applicant submits the cited art does not appear to teach or suggest at least "wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account delays caused by network topology" as recited in claim 6, in combination with the features of claim 1.

Applicant notes the cited art does not disclose, teach, or suggest at least "providing a Time Base selected by said processor, said Time Base being a baseline time value; determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips; transmitting each said offset for a local time counter to the chip with which the local time counter is associated; recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor" as recited in claim 10, in combination with the features of claim 1.

Applicant notes the cited art does not disclose, teach, or suggest at least "wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account delays caused by network topology" as recited in claim 27, in combination with the features of claim 22.

Applicant notes the cited art does not disclose, teach, or suggest at least "providing a Time Base selected by said processor, said Time Base being a baseline time value; determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips; transmitting each said offset for a local time counter to the chip with which the local time counter is associated; recording each offset associated with each said local time counter at a location accessible to the chip associated

with the local time counter; and normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor" as recited in claim 31, in combination with the features of claim 22.

G. New Claims

Applicant respectfully submits the cited art does not disclose, teach, or suggest at least "providing a baseline time value selected by a processor; detecting an error on a first chip, wherein the first chip is controlled by the processor; generating a first timestamp upon detecting the error on the first chip, wherein the first timestamp is generated by a first local time counter resident on the first chip; forwarding the first timestamp to the processor; normalizing the first timestamp with respect to the baseline time value; detecting an error on a second chip, wherein the second chip is controlled by the processor; generating a second timestamp upon detecting the error on the second chip, wherein the second timestamp is generated by a second local time counter resident on the second chip; forwarding the second timestamp to the processor; normalizing the second timestamp with respect to the baseline time value; and comparing the normalized first timestamp with the normalized second timestamp to determine if the error on the first chip occurred before the error on the second chip" as recited in new claim 36, or "wherein the processor normalizes the first timestamp after the first timestamp is forwarded to the processor" as recited in new claim 37.

H. Additional Remarks

Based on the above, Applicant submits that all of the claims are in condition for allowance. Favorable reconsideration is respectfully requested.

If any extension of time is required, Applicant hereby requests the appropriate extension of time. If any fees are inadvertently omitted or if any additional fees are required or have been overpaid, please appropriately charge or credit those fees to Meyertons, Hood, Kivlin, Kowert & Goetzel Deposit Account No. 50-1505/5681-97000/BNK.

Respectfully submitted,

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